



191935

STIC EIC 2100
Search Request Form

(10)

Today's Date:

6/5/06

What date would you like to use to limit the search?

Priority Date: 8/22/2003 Other:

Name GREG BENGTON
AU 2144 Examiner # 80501
Room # 4C79 Phone 23944
Serial # 10/646036

Format for Search Results (Circle One):

PAPER DISK EMAIL

Where have you searched so far?

USP DWPI EPO JPO ACM IBM TDB

IEEE INSPEC SPI Other _____

Is this a "Fast & Focused" Search Request? (Circle One) YES NO

A "Fast & Focused" Search is completed in 2-3 hours (maximum). The search must be on a very specific topic and meet certain criteria. The criteria are posted in EIC2100 and on the EIC2100 NPL Web Page at <http://ptoweb/patents/stic/stic-tc2100.htm>.

What is the topic, novelty, motivation, utility, or other specific details defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, definitions, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract, background, brief summary, pertinent claims and any citations of relevant art you have found.

Is this request for a BOARD of APPEALS case? (Circle One) YES NO

COPY MGT. SWITCH

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ATTACH 1

STIC Searcher EMORY DAMRON

Phone 2-3520

Date picked up 6/5/06

Date Completed 6/5/06

X COPY



P6 PUB 2005 0008016

Set	Items	Description
S1	998333	S SWITCH OR SWITCHES
S2	111643	S (ROUT? OR SWITCH?) (2N) (DEVICE? OR PERIPHERAL? OR APPARATUS? OR HARDWARE? OR COMPONENT? OR MODULE?)
S3	31086	S (ROUT? OR SWITCH?) (2N) (NODE? ? OR SUBCOMPONENT? OR ROUTER? OR APPLIANC? OR EQUIPMENT? OR HUB? ?)
S4	17011	S ROUTER?
S5	5194812	S STORE? OR STORAGE? OR ARCHIV? OR COPY? OR RECORD? OR REPLICAT? OR MIRROR?
S6	2180370	S MEMOR? OR CACHE? OR BUFFER? OR BACKUP? OR BACK?()UP OR DUPLICAT? OR PARALLEL?
S7	362602	S S1:S4 AND S5:S6
S8	29855	S ADDRESS? OR LOCATION? OR SECTOR? OR LOCALE? OR LOCALIT? OR NEIGHBORHOOD? OR ZONE?
S9	1009	S (STORAG? OR NETWORK? OR ETHERNET? OR INTRANET?) (3N) (ID OR IDS OR IDENT? OR LOCATER? OR LOCATOR? OR LABEL? OR POINTER?)
S10	108704	S SITE? ? OR REGION? OR PARTITION? OR SEGMENT? OR SECTION? OR LOCUS? OR POSITION? OR PLACE? OR AREA?
S11	113288	S CONVERT? OR CHANGE? OR CHANGING? OR MODIF? OR TRANSLAT? OR MODULAT? OR ALTER?
S12	30268	S TRANSFORM? OR ADAPT? OR MANIPULAT? OR AMEND? OR EDIT? OR UPDAT?
S13	35373	S REQUEST? OR QUERY? OR QUERIE? OR RETRIEV? OR INTERROGAT? OR FETCH? OR SEARCH? OR FIND? OR ACCESS?
S14	704	S LOOKUP? OR LOOK?()UP OR DATA() (MINE? OR MINING?) OR DATAMIN?
S15	112147	S ORIGINAL? OR 1ST OR FIRST? OR INITIAL? OR SOURCE? OR ISSUER? OR ISSUING? OR SEMINAL?
S16	47858	S PRIMARY? OR MASTER? OR MAIN OR CHIEF OR MANAGER? OR MANAGING? OR SUPERVIS? OR LEADER? OR HOST?
S17	60093	S NUMBER() (ONE OR 1) OR PRINCIPAL? OR LEAD OR CONTROLLER? OR HEAD
S18	57298	S FIRST? OR LEADOFF? OR INTRODUCTORY?
S19	180035	S COPY? OR MIRROR? OR BACKUP? OR COPY? OR RECORD? OR WRITE? OR WRITING? OR WRITTEN?
S20	73205	S REPLICAT? OR DUPLICAT? OR DOUBL? OR TWIN OR PARALLEL?
S21	91787	S SECOND? OR 2ND OR ANOTHER OR AUXILIAR? OR BACKUP? OR EXTRA OR SLAVE? OR SUPPLEMENT?
S22	50972	S SUBSIDIAR? OR DIFFERENT? OR ALTERNAT? OR NUMBER() (TWO OR 2) OR DESTINATION? OR TARGET? OR ENDPOINT?
S23	221283	S DATA? OR SAN(3N) (STOR? OR ACCESS? OR NETWORK?) OR SERVER? OR DEVICE? OR EQUIPMENT? OR COMPUTER?
S24	101017	S PROCESSOR? OR DATAPROCESSOR? OR MICROPROCESSOR? OR CPU? ? OR DATABASE? OR INFO?
S25	87467	S PERIPHERAL? OR APPARATUS? OR HARDWARE? OR COMPONENT? OR MODULE? OR NODE? OR APPLIANC?
S26	28251	S NETWORK? OR COMMUNICAT?()SYSTEM? OR NET? ?
S27	4858	S ETHERNET? OR INTERNET? OR INTRANET? OR EXTRANET?
S28	3724	S LAN? ? OR WAN? ? OR WAP? ? OR WLAN? ? OR VPN? ?
S29	61438	S IC=(H04L? OR G06F?)
S30	47544	S MC=(T01? OR W01?)
S31	329	S S7 AND S1:S4(5N) (S11:S12 AND S13:S14) AND (S15:S18 AND S19:S22) (5N) S23:
S32	197	S S31 AND (S26:S28 OR S28:S30)
S33	0	S S31 AND S11:S12(7N) 15:S18(7N) S13:S14 AND S11:S14(7N) (S15:S18 AND S19:S22)
S34	168	S S31 AND S15:S18(5N) S23:S25 AND S19:S22(5N) S23:S25
S35	255	S S32 OR S34
S36	73	S S35 AND AC=US/PR
S37	68	S S36 AND AY=(1970:2003)/PR
S38	67	S S36 NOT AY=(2004:2006)/PR
S39	182	S S35 NOT S36
S40	161	S S39 AND PY=1970:2003
S41	159	S S39 NOT PY=2004:2006

S42 231 S S37:S38 OR S40:S41
S43 231 IDPAT (sorted in duplicate/non-duplicate order)
S44 117 S S43 AND S1:S4(10N)S5:S6
S45 117 IDPAT (sorted in duplicate/non-duplicate order)
; show files

[File 347] **JAPIO** Dec 1976-2005/Dec(Updated 060404)
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[File 350] **Derwent WPIX** 1963-2006/UD,UM &UP=200635
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**File 350: Preview the enhanced DWPI through ONTAP DWPI (File 280). For more information, visit
<http://www.dialog.com/dwpi/>.*

45/3,K/43 (Item 43 from file: 350) Links
Derwent WPIX
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010410296 **Image available**
WPI Acc No: 1995-311645/199540
XRPX Acc No: N95-235332

Translating n-bit sequences into k-bit sequences with $k < n$
- uses RAMs, storing in first one n-bit words in order determined by
binary search key and second corresp. k-bit translations, both
addressed by same address established during search

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)

Inventor: LUIJTEN R P; SCHINDLER H R

Number of Countries: 018 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9523380	A1	19950831	WO 94EP538	A	19940225	199540 B
EP 746823	A1	19961211	EP 94909050	A	19940225	199703
			WO 94EP538	A	19940225	
JP 9503609	W	19970408	WO 94EP538	A	19940225	199724
			JP 95522084	A	19940225	
US 6023466	A	20000208	WO 94EP538	A	19940225	200014
			US 96702595	A	19960823	
EP 746823	B1	20000503	EP 94909050	A	19940225	200026
			WO 94EP538	A	19940225	
DE 69424315	E	20000608	DE 624315	A	19940225	200034
			EP 94909050	A	19940225	
			WO 94EP538	A	19940225	

Priority Applications (No Type Date): WO 94EP538 A 19940225

Patent Details:

Patent No Kind Lan Pg Main IPC Filing Notes

WO 9523380 A1 E 25 G06F-017/30

Designated States (National): JP US

Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL
PT SE

EP 746823 A1 E 25 G06F-017/30 Based on patent WO 9523380

Designated States (Regional): DE FR GB

JP 9503609 W 30 G11C-015/04 Based on patent WO 9523380

US 6023466 A H04L-012/56 Based on patent WO 9523380

EP 746823 B1 E G06F-017/30 Based on patent WO 9523380

Designated States (Regional): DE FR GB

DE 69424315 E G06F-017/30 Based on patent EP 746823

Based on patent WO 9523380

... storing in first one n-bit words in order determined by
binary search key and second corresp. k-bit translations, both
addressed by same address established during search

...Abstract (Basic): The translation apparatus has a first

memory (3) for storing in operation the n-bit sequences at first **addresses**, and a **second memory** (4) for storing the k-bit sequences at **second addresses** being directly derivable from and identical to the first addresses...

...An **address** register (6) **addresses** the two **memories**, and a comparator circuit (2) compares the output of the first **memory** with the n-bit sequence. The bits of the address register are set in accordance...

...of the comparator. The first addresses are determined by a binary search key. The two **memories** are random access **memories** (RAMs...

...ADVANTAGE - Provides low cost **storage**. Enables fast n-bit to k-bit **translation** for data **switches** for data throughput above 100 Mbps, especially for VCI/VPI translation...

...Title Terms: **STORAGE**;

International Patent Class (Main): **G06F-017/30**...

...**H04L-012/56**

International Patent Class (Additional): **G06F-012/00**...


Manual Codes (EPI/S-X): **T01-H01A**...

...**W01-A06B5A**...


...**W01-A06E1**...

...**W01-A06F**

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NETWORKWORLD

This story appeared on Network World at
<http://www.networkworld.com/news/tech/2003/0127techupdate.html>

Embedded switching adds reliability

Technology Update By Thomas Hammond-doel, Network World, 01/27/03

Embedded storage switching technology makes it feasible for storage systems to incorporate 2G bit/sec switched network connectivity within a storage array. Some benefits of embedded storage switching include much higher reliability, better performance and the ability to add drives without degrading performance.



Related links

Storage research center

The latest news, reviews, how-tos and more.

Storage: Picnic or panic?

How to keep storage from overwhelming you.

Buyer's Guide: Storage-area networks

The Storage Buzz

Technologies and trends shaping storage nets.

Graphic: How Embedded Storage Switching works

Shared bus architectures are used in the back end of many storage systems, rendering each disk or tape drive within the storage array a single point of failure. This dramatically increases the risk of an entire disk array going offline as the result of a problem with a single drive.

Whether the front end of a storage-area network or network-attached storage system uses Fibre Channel, iSCSI or IP, the storage system controller translates requests from the front end to the back end using the raw Fibre Channel Arbitrated Loop (FC-AL) shared bus protocol.

A new architecture

Arbitration and data flow of legacy FC-AL loops must progress through all devices in the loop. Each device along the path adds latency - and more importantly, an additional failure point that reduces reliability.

Legacy FC-AL loops operate through the mechanism of the controller, first arbitrating for control of the loop and then sending a command to a drive to prepare for data to be written to the drive or to request data from a specific location.

Back-end switching, however, uses the FC-AL protocol in a switched fashion, bringing point-to-point connectivity to each individual drive.

Embedded storage switching combines the crucial elements of complete integration of a crossbar switch core, embedded serializer/deserializers, 1- and 2-gigabaud bandwidth capabilities, and diagnostics to a single switch on a chip.

Storage systems physically arrange several disks into a single enclosure known as a Just a Bunch Of Disks (JBOD). Before the availability of the new level of integration brought by embedded storage switches, placing switching within a JBOD was impractical in modular storage systems because of real estate, power, heat and pricing issues. When embedded storage switching is added to a JBOD it becomes a Switched Bunch of Disks (SBOD).



Related links

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How to keep storage from overwhelming you.

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[The Storage Buzz](#)

Technologies and trends shaping storage nets.

Now when an initiator arbitrates for control of the system, instead of the arbitration proceeding through all the devices, such as in a shared bus architecture, the arbitration goes only to the switch matrix and back to the initiator. The process is very fast and greatly reduces system latency. After the initiator gains control, it can open the target drive and begin communications. Data packets sent between the initiator and drives are now point to point, and multiple conversations can take place at the same time.

Whether an embedded back-end switch provides connectivity from a controller to several JBODs or all the way to the individual hard disk drive using SBODs, embedded switching enables continuous reliability, availability and serviceability.

Embedded switching gives IT managers tools to deploy automatic maintenance, monitoring and repair. Each embedded storage switch port retimes the low-level signal, increasing signal integrity and reducing system jitter. Back-end embedded storage switches are in the ideal position to monitor traffic and signals, and to diagnose problems.

IT managers can establish policies at the highest level and be assured that those policies flow down to the lowest level of a storage system, where back-end embedded storage switches can implement them. For example, you might set a policy to automatically remove a hard drive upon detection of a failure trend, such as an increasing number of cyclic redundancy check errors over time.



Related links

Storage research center

The latest news, reviews, how-tos and more.

Storage: Picnic or panic?

How to keep storage from overwhelming you.

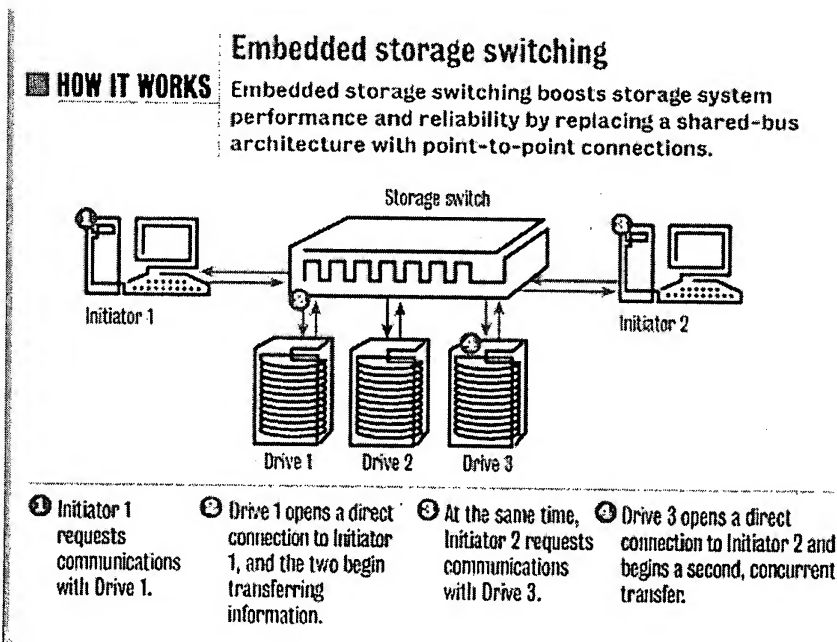
Buyer's Guide: Storage-area networks

The Storage Buzz

Technologies and trends shaping storage nets.

Embedded storage switching technology removes the performance bottlenecks that a shared-infrastructure storage system implementation imposes. All current topologies benefit from some aspect of back-end switching, where performance varies depending on the loading profile - from videostreaming to data-warehousing applications, and from lowered storage system cost of ownership and storage system automation.

Hammond-Doel is technical marketing director for Vixel. He can be reached at tom.hammond-doel@vixel.com.



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45/3,K/90 (Item 90 from file: 347) Links

JAPIO

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04332586 **Image available**

INFORMATION PROCESSING SYSTEM

Pub. No.: 05-324286 [JP 5324286 A]

Published: December 07, 1993 (19931207)

Inventor: SAITO TOSHIMITSU

MAMADA TORU

Applicant: TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)

Application No.: 04-173099 [JP 92173099]

Filed: June 30, 1992 (19920630)

Journal: Section: P, Section No. 1709, Vol. 18, No. 153, Pg. 30, March 14, 1994 (19940314) ...

Published: 19931207)

International Class: G06F-009/06; G06F-012/02

JAPIO Class: ...Memory Units)

ABSTRACT

PURPOSE: To effectively use **memory areas** which are accessible without requiring the control by CPU and to provide a common Operating... ..to be normally used from among the system control routines such as IRT routines are **stored** in a **1st memory 25** in the **CPU address** space, and parts not to be normally used from among the system control routines are **stored** in a **2nd memory 31** allocated outside the **CPU address** space. Normally, a **changing switch 27** connects the **1st memory 25** to a bus 11, and connects the **2nd memory 31** to the bus 11 under the control of the CPU 13. In executing the control processing routines not to be normally used, the CPU 13 controls the circuit **changing switch 27** to connect the **2nd memory 31** to the bus, processing the control routine **stored** in the **2nd memory 31**. The dissimilar parts of respective OSs are **stored** in the **2nd memory 31** according to the specifications of each, and the OS supplied from outside may be...

INFORMATION PROCESSING SYSTEM

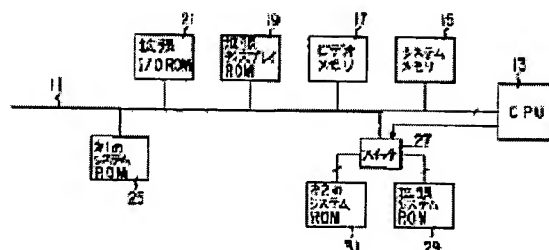
Patent number: JP5324286
Publication date: 1993-12-07
Inventor: SAITO TOSHIMITSU; MAMADA TORU
Applicant: TOKYO SHIBAURA ELECTRIC CO
Classification:
- international: G06F9/06; G06F9/445; G06F12/02; G06F12/06;
G06F9/06; G06F9/445; G06F12/02; G06F12/06; (IPC1-7): G06F9/06; G06F12/02
- european:
Application number: JP19920173099 19920630
Priority number(s): JP19920173099 19920630; JP19920062377 19920318

Report a data error here

Abstract of JP5324286

PURPOSE: To effectively use memory areas which are accessible without requiring the control by CPU and to provide a common Operating System(OS) between computers with dissimilar specifications.

CONSTITUTION: Parts to be normally used from among the system control routines such as IRT routines are stored in a 1st memory 25 in the CPU address space, and parts not to be normally used from among the system control routines are stored in a 2nd memory 31 allocated outside the CPU address space. Normally, a changing switch 27 connects the 1st memory 25 to a bus 11, and connects the 2nd memory 31 to the bus 11 under the control of the CPU 13. In executing the control processing routines not to be normally used, the CPU 13 controls the circuit changing switch 27 to connect the 2nd memory 31 to the bus, processing the control routine stored in the 2nd memory 31. The dissimilar parts of respective OSs are stored in the 2nd memory 31 according to the specifications of each, and the OS supplied from outside may be commonly used.



Data supplied from the esp@cenet database - Worldwide

45/3,K/53 (Item 53 from file: 350) Links

Derwent WPIX

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008883153 **Image available**

WPI Acc No: 1992-010422/199202

XRPX Acc No: N92-008000

**Microcontroller with bank switching memory - permits
program to automatically cross memory bank boundaries without user
intervention**

Patent Assignee: MOTOROLA INC (MOTI)

Inventor: CATHERWOOD M I; LIVINGSTON K; NASH J C

Number of Countries: 005 Number of Patents: 006

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 465248	A	19920108	EP 91306078	A	19910704	199202	B
EP 465248	A3	19920304	EP 91306078	A	19910704	199325	
US 5249280	A	19930928	US 90548695	A	19900705	199340	
EP 465248	B1	20000119	EP 91306078	A	19910704	200009	
DE 69131919	E	20000224	DE 631919	A	19910704	200017	
			EP 91306078	A	19910704		
JP 3233163	B2	20011126	JP 91183957	A	19910628	200201	

Priority Applications (No Type Date): US 90548695 A 19900705

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
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EP 465248	A		13		
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Designated States (Regional): DE FR GB

US 5249280	A		12	G06F-012/00	
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EP 465248	B1	E		G06F-012/06	
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Designated States (Regional): DE FR GB

DE 69131919	E			G06F-012/06	Based on patent EP 465248
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JP 3233163	B2		9	G06F-012/06	Previous Publ. patent JP 4233640
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Microcontroller with bank switching memory - ...

**...permits program to automatically cross memory bank boundaries
without user intervention**

...Abstract (Basic): has a processor (30) for executing a number of instructions and for communicating with external **memory**, and is subdivided into a predetermined number of **memory** banks, via a communication bus (49). Each one of the **memory** banks is defined by a boundary of **memory** addresses, a **memory** bank **switch** (90) for **accessing** a selected **memory** bank in the external **memory**. The system comprises a register (92 and 94) for storing a number of **memory** addresses, with each one comprising a first set of **address** bits corresponding to a selected **memory** bank, and a **second** set of **address** bits corresponding to a **memory** location in the selected

memory bank...

- ...An adder unit (98), coupled to the register, adds a **memory address stored** in the register to an offset address, and provides an extended address to the communications bus, and then selectively updates the first set of **address bits** of the **memory address**, via an internal communications bus when the extended address exceeds the boundary of **addresses** for the selected **memory bank...**
- ...ADVANTAGE - Executes a number of instructions and communicates with external **memory** via a communication bus. (13pp Dwg.No.6/6)
- ...Abstract (Equivalent): has a processor for executing a number of instructions and for communicating with an external **memory** that is subdivided into a specific number of **memory banks**. A **memory bank switching device** for accessing a selected **memory bank** in the external **memory** comprises a register for storing a number of **memory addresses**, wherein each one of the **memory addresses** comprises a first set of **address bits** corresp. to a unique **memory bank**, and a **second** set of **address bits** corresp. to a **memory location** in the unique **memory bank...**
- ...A **first device** is coupled to the register, for adding a **memory address stored** in the register to an offset address. The **first device** provides an extended **memory address** to the communications bus, and selectively updates the first set of **address bits**, of the **memory address**, via an internal communications bus, when the extended **memory address** exceeds the boundary of **memory addresses** for the unique **memory bank**, to allow the processor to cross the boundary of **memory addresses** for the unique **memory bank** to access information **stored** at the extended **memory address**.
...
- ...ADVANTAGE - Permits program to automatically cross **memory bank** boundaries, without user intervention
- ...Title Terms: **SWITCH**;
- International Patent Class (Main): **G06F-012/00...**
- ...**G06F-012/06**
- International Patent Class (Additional): **G06F-012/02**
- Manual Codes (EPI/S-X): **T01-H01A...**
- ...**T01-H03C**

45/3,K/30 (Item 30 from file: 350) Links
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011971591 **Image available**
WPI Acc No: 1998-388501/199833
XRPX Acc No: N98-302908

**Queuing system for broadband multi-media satellite and
terrestrial communications network - has first
storage device for holding data cells received at
switch inputs, and switch has address
translation device for assigning destination to each
cell, and second storage cell for holding
destination data**

Patent Assignee: NORTHERN TELECOM LTD (NELE)
Inventor: ABU-AMARA H H; KOTAMARTI V
Number of Countries: 019 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 9829993	A1	19980709	WO 97US24217	A	19971229	199833 B
US 5870396	A	19990209	US 96775275	A	19961231	199913

Priority Applications (No Type Date): US 96775275 A 19961231
Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
WO 9829993	A1	E	68 H04L-012/56	
Designated States (National): CA US				
Designated States (Regional): AT BE CH DE DK ES FI FR GB GR IE IT LU MC				
NL PT SE				
US 5870396	A		H04L-012/56	

**Queuing system for broadband multi-media satellite and
terrestrial communications network - ...**

**...has first storage device for holding data
cells received at switch inputs, and switch has
address translation device for assigning
destination to each cell, and second storage cell
for holding destination data**

**...Abstract (Basic): The apparatus for routing data packets
has a number of inputs for...**

**...receiving the packets. A first storage device
stores the data**

...

**...be stored within each segment within the number of
segments. An...**

...**address translation device** assigns a **destination**
from a number...

...of **destinations** to each **data** packet received at the inputs
...

...A **second storage device** has a number of
sections, each being...

...number of **segments**. The **second storage**
device stores location
...

...associated with the **destination** assigned to the **data**
packet in...

...the **first storage device**. A reading **device**
transfers data packets...

...from the **first storage device** to the number of
destinations using...

...insensitive to **network** size

...Title Terms: **NETWORK**;

International Patent Class (Main): **H04L-012/56**

Manual Codes (EPI/S-X): **W01-B05A1A**...

45/3,K/11 (Item 11 from file: 350) Links
Derwent WPIX
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015903249 **Image available**
WPI Acc No: 2004-061089/200406
XRPX Acc No: N04-049488

**Direct memory access transfers changing and
overlapping method for server, involves conducting access transfer in
response to detected another access transfer**

Patent Assignee: HEPNER D F (HEPN-I); WALLS A D (WALL-I)

Inventor: HEPNER D F; WALLS A D

Number of Countries: 001 Number of Patents: 001

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030229733	A1	20031211	US 2002163288	A	20020605	200406 B

Priority Applications (No Type Date): US 2002163288 A 20020605

Patent Details:

Patent No	Kind	Lan Pg	Main IPC	Filing Notes
US 20030229733	A1	13	G06F-013/28	

**Direct memory access transfers changing and
overlapping method for server, involves conducting access transfer in
response to...**

Abstract (Basic):

... The method involves detecting a direct **memory** access
(DMA) transfer by detecting access to a **memory location**
corresponding to the DMA transfer by a DMA transfer detector. A
target address is compared with a **memory** access
address. Another DMA transfer is conducted in response to
the detected DMA transfer. The DMA transfers are...

... Used for changing and overlapping DMA transfers in **server**
, **storage** controller, host adaptor, network **routers**, and
data switches.

...

...The method facilitates **parallel** execution of DMA transfers to
increase the systems throughput while reducing data latency and permits
...

...The drawing shows a schematic block diagram of data **networking**
system...

...Data **networking** system (300...

...**Storage** arrays (340...

...Storage area networks (350
...Title Terms: MEMORY;
International Patent Class (Main): G06F-013/28
Manual Codes (EPI/S-X): T01-H05B2...

...T01-N02A3C...

...T01-N02B1

Set	Items	Description
S1	307215	S SWITCH OR SWITCHES
S2	44667	S (ROUT? OR SWITCH?) (2N) (DEVICE? OR PERIPHERAL? OR APPARATUS? OR HARDWARE? OR COMPONENT? OR MODULE?)
S3	68908	S (ROUT? OR SWITCH?) (2N) (NODE? ? OR SUBCOMPONENT? OR ROUTER? OR APPLIANC? OR EQUIPMENT? OR HUB? ?)
S4	40688	S ROUTER?
S5	4619676	S STORE? OR STORAGE? OR ARCHIV? OR COPY? OR RECORD? OR REPLICAT? OR MIRROR?
S6	2345428	S MEMOR? OR CACHE? OR BUFFER? OR BACKUP? OR BACK? ()UP OR DUPLICAT? OR PARALLEL?
S7	30863	S S1:S4(10N)S5:S6
S8	2901	S ADDRESS? OR LOCATION? OR SECTOR? OR LOCALE? OR LOCALIT? OR NEIGHBORHOOD? OR ZONE?
S9	75	S (STORAG? OR NETWORK? OR ETHERNET? OR INTRANET?) (3N) (ID OR IDS OR IDENT? OR LOCATER? OR LOCATOR? OR LABEL? OR POINTER?)
S10	5783	S SITE? ? OR REGION? OR PARTITION? OR SEGMENT? OR SECTION? OR LOCUS? OR POSITION? OR PLACE? OR AREA?
S11	7174	S CONVERT? OR CHANGE? OR CHANGING? OR MODIF? OR TRANSLAT? OR MODULAT? OR ALTER?
S12	3768	S TRANSFORM? OR ADAPT? OR MANIPULAT? OR AMEND? OR EDIT? OR UPDAT?
S13	4945	S REQUEST? OR QUERY? OR QUERIE? OR RETRIEV? OR INTERROGAT? OR FETCH? OR SEARCH? OR FIND? OR ACCESS?
S14	412	S LOOKUP? OR LOOK? ()UP OR DATA() (MINE? OR MINING?) OR DATAMIN?
S15	6514	S ORIGINAL? OR 1ST OR FIRST? OR INITIAL? OR SOURCE? OR ISSUER? OR ISSUING? OR SEMINAL?
S16	3193	S PRIMARY? OR MASTER? OR MAIN OR CHIEF OR MANAGER? OR MANAGING? OR SUPERVIS? OR LEADER? OR HOST?
S17	2104	S NUMBER() (ONE OR 1) OR PRINCIPAL? OR LEAD OR CONTROLLER? OR HEAD
S18	3495	S FIRST? OR LEADOFF? OR INTRODUCTORY?
S19	7175	S COPY? OR MIRROR? OR BACKUP? OR COPY? OR RECORD? OR WRITE? OR WRITING? OR WRITTEN?
S20	9997	S REPLICAT? OR DUPLICAT? OR DOUBL? OR TWIN OR PARALLEL? OR REPLICA? ?
S21	3784	S SECOND? OR 2ND OR ANOTHER OR AUXILIAR? OR BACKUP? OR EXTRA OR SLAVE? OR SUPPLEMENT?
S22	6587	S SUBSIDIAR? OR DIFFERENT? OR ALTERNAT? OR NUMBER() (TWO OR 2) OR DESTINATION? OR TARGET? OR ENDPOINT?
S23	18336	S DATA? OR SAN(3N) (STOR? OR ACCESS? OR AREA? OR NETWORK?) OR SERVER? OR DEVICE? OR EQUIPMENT? OR COMPUTER?
S24	6854	S PROCESSOR? OR DATAPROCESSOR? OR MICROPROCESSOR? OR CPU? ? OR DATABASE? OR INFO?
S25	9110	S PERIPHERAL? OR APPARATUS? OR HARDWARE? OR COMPONENT? OR MODULE? OR NODE? OR APPLIANC?
S26	13696	S NETWORK? OR COMMUNICAT? ()SYSTEM? OR NET? ?
S27	2030	S ETHERNET? OR INTERNET? OR INTRANET? OR EXTRANET?
S28	749	S LAN? ? OR WAN? ? OR WAP? ? OR WLAN? ? OR VPN? ?
S29	22	S S7 AND S1:S4(7N)S11:S12(7N)S13:S14 AND (S15:S18 AND S19:S22) (10N)S23:S25
S30	14	S S29 AND S26:S28
S31	260	S S7 AND S8:S10 AND S11:S12 AND S13:S14 AND S15:S18 AND S19:S22
S32	226	S S31 AND S23:S25
S33	167	S S31 AND S26:S28
S34	265	S S29:S33
S35	186	S S34 AND PY=1970:2003
S36	201	S S34 NOT PY=2004:2006
S37	201	S S35:S36
S38	157	RD (unique items)

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00144617 **Document Type:** Review

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...connections. Embedded storage switching technology makes it possible for storage systems to include 2Gbps switched network connectivity within a storage array. Advantages include high reliability, better performance, and the ability to add drives without impacting performance. Whether the front end of a storage area network (SAN) or network-attached storage system (NAS) uses Fibre Channel, iSCSI, or IP, the storage system controller translates requests from the front end to the back end using the undiluted Fibre Channel Arbitrated Loop (FC-AL) shared bus protocol. With embedded storage switching, an initiator requests communication with drive 1, and drive 1 opens a direct connection to Initiator 1, and the two start transferring information. Concurrently, initiator 2 requests communications with drive 3, and drive 3 then opens a direct connection to initiator 2 and starts a second, concurrent transfer. Embedded storage switching provides IT managers with tools for deploying automatic maintenance, monitoring, and repair, and they also can establish policies... ..level and rest assured that those policies flow down to the lowest level of a storage system, where back-end embedded storage switches can deploy them.

Descriptors: Communications Interfaces; Embedded Systems; Hardware Selection
1999